Docket No.: P2001,0158

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

By: _____ Date: December 31, 2003

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applic. No.	:	10/657,928
Applicant	:	Wolfgang Gustin et al.
Filed	:	September 10, 2003
Art Unit	:	to be assigned
Examiner	:	to be assigned
Docket No.	:	P2001,0158
Customer No.	:	24131

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner for Patents

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

L. Nesbit et al.: "A 0.6 μm^2 256Mb Trench DRAM Cell With Self-Aligned BuriEd STrap (BEST)", *IEDM 1993, pp. 627-630*;

G. Bronner et al.: "A Fully planarized 0.25µm CMOS Technology for 256Mbit DRAM and Beyond", *1995 Symposium on VLSI Technology Digest of technical Papers, Kyoto, Japan, pp. 15-16*;

Stanley Wolf: "Silicon Processing For The VLSI Era – Volume 2: Process Integration", *Lattice Press, Sunset Beach, California, cover page only*;

D. Widmann et al.: "Technologie hochintegrierter Schaltungen", *Springer Verlag, Heidelberg, Germany, 2nd ed., cover page only*;

U. Gruening et al.: A Novel Trench DRAM Cell with a VERtIcal Access Transistor and BuriEd Strap (VERI BEST) for 4Gb/16Gb", *IEEE, 1999, 4 pp*. This reference had been submitted in an earlier IDS and the word "trench" had been omitted from the title inadvertently. The Examiner is kindly requested to make the change.

Respectfully submitted,

Gregory L. Mayback
Reg. No. 40,719

For Applicants

Date: December 31, 2003

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FORM PTO-1449 (SUBSTITUTE)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(37 CFR 1.98(b))

Attorney Docket No.:	Applic. No.
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September 10, 2003	

U.S. PATENT DOCUMENTS

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	O	L. Nesbit et al.: "A 0.6 μm^2 256Mb Trench DRAM Cell With Self-Aligned BuriEd STrap (BEST)", *IEDM 1993, pp. 627-630*
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EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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